What is Claimed is:

1. A semiconductor memory device comprising:

an input buffer for detecting a logic level of an address inputted by using a reference voltage;

an address latch for latching an address outputted from the input buffer, and for sequentially outputting a bank selecting signal, a row address and a column address;

a nonvolatile ferroelectric mode register for programming parameters on a chip operation in a nonvolatile ferroelectric capacitor, and for outputting a control signal to control a synchronization operation of a cell array depending on a programmed code; and

a bank array, comprising a plurality of cell arrays, controlling read/write operations of one cell array synchronously with respect to the control signal in response to the bank selecting signal, the row address and the column address.

2. The device according to claim 1, wherein the logic level of the address detected in the input buffer is a stub series terminated transceiver logic level.

3. The device according to claim 1, wherein the

input buffer comprises:

a differential amplifier for comparing and amplifying voltage levels of the reference voltage and the address when a differential amplification enable signal is enabled; and

a driver for precharging an output signal of the differential amplifier to a power voltage when the differential amplification enable signal is disabled.

4. The device according to claim 1, wherein the address latch comprises:

a column address latch for latching an address outputted from the input buffer, and for outputting the column address when a column address strobe signal is activated;

a row address latch for latching an address outputted from the input buffer, and for outputting the row address when a row address strobe signal is activated; and

a bank selector for latching an address outputted from the input buffer, and for outputting the bank selecting signal and the bank address when the row address strobe signal is activated.

5. The device according to claim 1, wherein the

input buffer comprises:

a column address buffer for detecting a logic level of a column address inputted by the reference voltage;

a row address buffer for detecting a logic level of a row address inputted by the reference voltage; and

a bank address buffer for detecting a logic level of a bank address inputted by the reference voltage.

6. The device according to claim 5, further comprising a switching controller for selectively switching an output paths of the column address buffer, the row address buffer and the bank address buffer depending on the programmed code in the nonvolatile ferroelectric capacitor, and for time-divisionary controlling the bank address, the row address and the column address sequentially.

7. The device according to claim 6, wherein the switching controller comprises:

a first switching controller for selectively controlling an output paths of the column address buffer and the row address buffer in response to a first switching control signal generated depending on a programmed code in a first nonvolatile ferroelectric capacitor; and

a second switching controller for selectively

controlling an output paths of the row address buffer and the bank address buffer in response to a second switching control signal generated depending on a programmed code in a second nonvolatile ferroelectric capacitor.

8. The device according to claim 7, wherein the first switching controller comprises:

a first controller, comprising the first nonvolatile ferroelectric capacitor, generating the first switching control signal;

a first switching unit for selecting an output path of the column address buffer when the first switching control signal is activate; and

a second switching unit for selecting an output path of the row address buffer when the first switching control signal is inactivated.

9. The device according to claim 7, wherein the second switching controller comprises:

a second controller, comprising the second nonvolatile ferroelectric capacitor, for generating the second switching control signal;

a third switching unit for selecting an output path of the bank address buffer when the second switching

control signal is activated; and

a fourth switching unit for selecting an output path of the row address buffer when the second switching control signal is inactivated.

10. The device according to claim 1, comprising:

an address transition detector for detecting transition of the row address and the bank address, and for activating an address transition detecting signal when at least one of addresses transits;

a column burst counter for counting the column address synchronously with respect to the control signal in a burst mode;

a control signal generator for selectively generating driving control signals necessary for the chip operation depending on control of the nonvolatile ferroelectric mode register;

a delay-locked loop for generating a clock of the same waveform having a phase difference synchronously with respect to a clock signal applied to the control signal generator;

a data strobe buffer for outputting a data strobe signal to control data output synchronously with respect to the clock;

a data input buffer for comparing input data with the reference voltage and outputting the comparison result into the bank array; and

a data output buffer for outputting data stored in the cell array synchronously with respect to the data strobe signal.

11. The device according to claim 1, further comprising a termination resistance regulator, located between the input buffer and an input pin, for selectively controlling termination resistance of an input signal inputted through the input pin depending on the programmed code in the nonvolatile ferroelectric capacitor.

12. The device according to claim 11, wherein the termination resistance regulator comprises:

a first nonvolatile ferroelectric register for selectively outputting a first switching driving signal and a second switching driving signal to control the termination resistance depending on data set in the nonvolatile ferroelectric capacitor;

a first termination switching unit, switched in response to the first switching driving signal, for selectively supplying a termination voltage; and

a second termination switching unit, switched in response to the second switching driving signal, for selectively supplying a ground voltage.

13. The device according to claim 12, wherein the termination resistance regulator further comprises:

a first termination resistor, located between the first termination switching unit and a supply node of the input signal, for controlling a transmission characteristic of the input signal; and

a second termination resistor, located between the second termination switching unit and a supply node of the input signal, for controlling a transmission characteristic of the input signal.

14. The device according to claim 11, wherein the termination resistance regulator comprises:

a second nonvolatile ferroelectric register for selectively outputting a third switching driving signal and a fourth switching driving signal to control the termination resistance depending on data set in the nonvolatile ferroelectric capacitor;

a first termination controller for performing a logic operation on the third switching driving signal and a first

chip driving control signal;

a third termination switching unit, switched by control of the first termination controller, for selectively supplying a termination voltage;

a second termination controller for performing a logic operation one the fourth switching driving switching driving signal and a second chip driving control signal; and

a fourth termination switching unit, switched by control of the second termination controller, for selectively supplying a ground voltage.

15. The device according to claim 14, wherein the termination resistance regulator further comprises:

a third termination resistor, located between the third termination switching unit and a supply node of the input signal, for controlling a transmission characteristic of the input signal; and

a fourth termination resistor, located between the fourth termination switching unit and a supply node of the input signal, for controlling a transmission characteristic of the input signal.

16. The device according to claim 1, wherein the

nonvolatile ferroelectric mode register comprises:

a program command processor for sequentially outputting a plurality of multiple command signals to code a program command in response to a write enable signal, a row address strobe signal, a column address strobe signal and a reset signal;

a program register controller for performing a logic operation on the plurality of multiple command signals and a power-up detecting signal, and outputting a write control signal and a cell plate signal;

a program register array, comprising the nonvolatile ferroelectric capacitor, for outputting the control signal set in the nonvolatile ferroelectric capacitor in response to the write control signal and the cell plate signal; and

a reset circuit unit for outputting the reset signal into the program register controller in a power-up mode.

17. A semiconductor memory device comprising:

an address latch for latching an inputted address, and outputting a bank selecting signal, a row address and a column address sequentially;

a nonvolatile ferroelectric mode register for programming parameters on a chip operation in a nonvolatile ferroelectric capacitor, and outputting a control signal to

control a synchronization operation of a cell array depending on the programmed code; and

a bank array, comprising a plurality of cell arrays, for controlling read/write operations of one cell array synchronously with respect to the control signal in response to the bank selecting signal, the row address and the column address.

18. The device according to claim 17, wherein the logic level of the address is a low voltage transistortransistor logic level.

19. The device according to claim 17, wherein the address latch comprises:

a column address latch for latching the address, and outputting the column address when a column address strobe signal is activated;

a row address latch for latching the address, and outputting the row address when a row address strobe signal is activated; and

a bank selector for latching the address, and outputting the bank selecting signal and the bank address when the row address strobe signal is activated.

20. The device according to claim 17, further comprising a switching controller for selectively switching an output path of the address depending on the programmed code in the nonvolatile ferroelectric capacitor, and for sequentially and time-divisionary controlling the bank address, the row address and the column address.

21. The device according to claim 20, wherein the switching controller comprises:

a first switching controller for selectively controlling output paths of the column address and the row address in response to a first switching control signal generated by a programmed code in a first nonvolatile ferroelectric capacitor; and

a second switching controller for selectively controlling output paths of the row address and the bank address in response to a second switching control signal generated by a programmed code in a second nonvolatile ferroelectric capacitor.

22. The device according to claim 21, wherein the first switching controller comprises:

a first controller, comprising the first nonvolatile ferroelectric capacitor, for generating the first switching

control signal;

a first switching unit for selecting an output path of the column address when the first switching control signal is activated; and

a second switching unit for selecting an output path of the row address when the first switching control signal is inactivated.

23. The device according to claim 21, wherein the second switching controller comprises:

a second controller, comprising the second nonvolatile ferroelectric capacitor, for generating the second switching control signal;

a third switching unit for selecting an output path of the bank address when the second switching control signal is activated; and

a fourth switching unit for selecting an output path of the row address when the second switching control signal is inactivated.

24. The device according to claim 17, comprising:

an address transition detector for detecting transitions of the row address and the bank address, and for activating an address transition detecting signal when

at least one of addresses transits;

a column burst counter for counting the column address synchronously with respect to the control signal in a burst mode;

a control signal generator for selectively generating driving control signals necessary for the chip operation depending on control of the nonvolatile ferroelectric mode register; and

a data input/output buffer for controlling data input/output with the cell array.

25. The device according to claim 17, further comprising a termination resistance regulator, located between the address latch and an input pin, for selectively controlling a termination resistance of an input signal inputted through the input pin depending on a programmed code in a nonvolatile ferroelectric capacitor.

26. The device according to claim 25, wherein the termination resistance regulator comprises:

a first nonvolatile ferroelectric register for selectively outputting a first switching driving signal and a second switching driving signal to control the termination resistance depending on data set in the

nonvolatile ferroelectric capacitor;

a first termination switching unit, switched in response to the first switching driving signal, for selectively outputting a termination voltage; and

a second termination switching unit, switched in response to the second switching driving signal, for selectively supplying a ground voltage.

27. The device according to claim 26, wherein the termination resistance regulator further comprises:

a first termination resistor, located between the first termination switching unit and a supply node of the input signal, for controlling a transmission characteristic of the input signal of the input signal; and

a second termination resistor, located between the second termination switching unit and a supply node of the input signal, for controlling a transmission characteristic of the input signal.

28. The device according to claim 25, wherein the termination resistance regulator comprises:

a second nonvolatile ferroelectric register for selectively outputting a third switching driving signal and a fourth switching driving signal to control the

termination resistance depending on data set in the nonvolatile ferroelectric capacitor;

a first termination controller for performing a logic operation on the third switching driving signal and a first chip driving control signal;

a third termination switching unit, switched by control of the first termination controller, for selectively supplying a termination voltage;

a second termination controller for performing a logic operation on the fourth switching driving signal and a second chip driving control signal; and

a fourth termination switching unit, switched by control of the second termination controller, for selectively supplying a ground voltage.

29. The device according to claim 28, wherein the termination resistance regulator further comprises:

a third termination resistor, located between the third termination switching unit and a supply node of the input signal, for controlling a transmission characteristic of the input signal; and

a fourth termination resistor, located between the fourth termination switching unit and a supply node of the input signal, for controlling a transmission characteristic

of the input signal.

30. The device according to claim 17, wherein the nonvolatile ferroelectric mode register comprises:

a program command processor for sequentially outputting a plurality of multiple command signals to code a program command in response to a write enable signal, a row address strobe signal, a column address strobe signal and a reset signal;

a program register controller for performing a logic operation on the plurality of multiple command signal and a power-up detecting signal, and outputting a write control signal and a cell plate signal;

a program register array, comprising the nonvolatile ferroelectric capacitor, for outputting the control signal set in the nonvolatile ferroelectric capacitor in response to the write control signal and the cell plate signal; and

a reset circuit unit for outputting the reset signal into the program register controller in a power-up mode.

31. A semiconductor memory device comprising:

a nonvolatile ferroelectric mode register, comprising a nonvolatile ferroelectric memory, for outputting a control signal to control a synchronization operation of a

cell array depending on a programmed mode register value in the nonvolatile ferroelectric memory; and

a bank array, comprising a plurality of cell arrays, for performing read/write operations of the selected cell array synchronously with respect to the control signal.